Amendments to the Specification begin on page 3 of this paper.

Amendments to the Claims are reflected in the listing of the Claims which begins on page 4 of this paper.

Remarks/Arguments begin on page 18 of this paper.

Amendments to the Specification

Please amend the second paragraph on page 9 as follows:

Solder pads 30 ~~31~~ are formed to connect the capacitor electrodes 34 to the metal segments Vdd and Vss. The capacitor 38 serves as a local power reservoir to decouple the external power ground noise caused by the wirebonds 26 and 28 and other system components. A decoupling capacitor is connected in association with each of at least two wirebonds.

Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1. (currently amended) An integrated ~~A~~ circuit chip ~~component~~ comprising:

a semiconductor substrate;

a transistor in and over ~~on~~ said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers;

a power metal structure ~~bus~~ over said passivation layer, wherein said power metal structure comprises a copper layer; ~~semiconductor substrate;~~

a ground metal structure ~~bus~~ over said passivation layer, wherein said ground metal structure comprises a copper layer; ~~semiconductor substrate;~~

a capacitor over said passivation layer; ~~semiconductor substrate;~~

a first solder connection connecting said capacitor to said power metal structure; ~~bus;~~ and

a second solder connection connecting said capacitor to said ground metal structure. ~~bus.~~

Claims 2 and 3 (canceled)

4. (withdrawn - currently amended) The integrated circuit chip ~~component~~ according to claim 1 further comprising a polymer layer over said passivation layer, ~~semiconductor substrate,~~ wherein said power and ground metal structures are ~~bus is~~ on said polymer layer.

Claims 5 and 6 (canceled)

7. (currently amended) The integrated circuit chip ~~component~~ according to claim 1, wherein said ground metal structure comprises a ~~power bus comprises~~ gold layer over said copper layer.

Claim 8 (canceled)

9. (currently amended) An integrated ~~A~~ circuit chip ~~component~~ comprising:

a semiconductor substrate;

a transistor in and over ~~on~~ said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

~~a first contact pad over said semiconductor substrate;~~

a passivation layer over said multiple metal and dielectric layers, ~~semiconductor substrate,~~ a first opening in said passivation layer exposing ~~a top surface of said~~ a first contact pad of said multiple metal and dielectric layers, wherein said passivation layer comprises nitride;

a second contact pad connected to said first contact pad through said first opening, ~~top surface,~~ wherein the position of said second contact pad from a top perspective view is different from that of said first contact pad, wherein said second contact pad comprises a gold layer; ~~and~~

a capacitor over said passivation layer; and ~~, wherein said capacitor is connected to said second contact pad.~~

a solder connection connecting said capacitor to said second contact pad.

10. (currently amended) The integrated circuit chip ~~component~~ according to claim 9 further comprising a third contact pad exposed by a second opening in said passivation layer, and a wirebond on said third contact pad.

11. (currently amended) The integrated circuit chip ~~component~~ according to claim 9 further comprising a third contact pad over said passivation layer, and a wirebond on said third contact pad.

12. (currently amended) The integrated circuit chip ~~component~~ according to claim 9 further comprising a third contact pad exposed by a second opening in said passivation layer, a fourth contact pad on said third contact pad, and a wirebond on said fourth contact pad.

13. (currently amended) The integrated circuit chip ~~component~~ according to claim 9, wherein said gold layer has a thickness of greater than 1 micron. ~~further comprising a solder connecting said capacitor to said second contact pad.~~

14. (currently amended) The integrated circuit chip ~~component~~ according to claim 9, wherein said second contact pad comprises a copper layer under said gold layer.

15. (currently amended) An integrated ~~A~~ circuit chip ~~component~~ comprising:

a semiconductor substrate;

a transistor in and over ~~on~~ said semiconductor substrate;

multiple metal and dielectric layers over said semiconductor substrate;

a passivation layer over said multiple metal and dielectric layers;

a first metal pad over said semiconductor substrate;

a second metal pad having a portion over said passivation layer, ~~semiconductor substrate,~~ wherein said second metal pad is used to be wirebonded thereto;

a capacitor over said passivation layer; ~~semiconductor substrate;~~ and

a solder connection connecting said capacitor to said first metal pad.

16. (currently amended) The integrated circuit chip ~~component~~ according to claim 15 further comprising a wirebond on said second metal pad, wherein said wirebond comprises gold.

17. (currently amended) The integrated circuit chip ~~component~~ according to claim 15, wherein said first metal pad comprises a gold layer.

18. (currently amended) The integrated circuit chip ~~component~~ according to claim 15,

wherein said first metal pad comprises a copper layer.

19. (currently amended) The integrated circuit chip ~~component~~ according to claim 15 further comprising a ground metal structure ~~bus~~ connected to said capacitor.

20. (currently amended) The integrated circuit chip ~~component~~ according to claim 15, ~~16,~~ wherein said capacitor is connected to said second metal pad. ~~wirebond.~~

21. (currently amended) The integrated circuit chip ~~component~~ according to claim 15 further comprising a power metal structure ~~bus~~ connected to said capacitor.

22. (currently amended) The integrated circuit chip ~~component~~ according to claim 15, wherein said first metal pad is over said passivation layer. ~~further comprising a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, and a second metallization structure over said passivation layer, wherein said second metallization structure is provided with said first metal pad.~~

23. (currently amended) The integrated circuit chip ~~component~~ according to claim 15 ~~16~~ further comprising ~~a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, and~~ a ~~second~~ metallization structure over said passivation layer, wherein said capacitor is connected to said second metal pad ~~wirebond~~ through said ~~second~~ metallization structure.

Claim 24 (canceled)

25. (currently amended) The integrated circuit chip ~~component~~ according to claim 15, ~~further comprising a passivation layer over said semiconductor substrate, wherein said second metal pad is exposed by an opening in said passivation layer and~~ wherein said passivation layer comprises silicon nitride.

26. (currently amended) The integrated circuit chip ~~component~~ according to claim 15 further comprising a third metal pad over said semiconductor substrate, ~~and a passivation layer over said semiconductor substrate,~~ an opening in said passivation layer exposing said third metal pad, wherein said second metal pad is over ~~on~~ said third metal pad ~~and wherein said passivation layer comprises nitride~~.

27. (currently amended) The integrated circuit chip ~~component~~ according to claim 15, wherein said second metal pad comprises gold.

Claim 28 (canceled)

29. (withdrawn - currently amended) The integrated circuit chip ~~component~~ according to claim 15 further comprising ~~a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure,~~ a polymer layer over said passivation layer, ~~and a second metallization structure over said polymer layer,~~ wherein said first metal pad is on said polymer layer. ~~second metallization structure is~~

~~provided with said first metal pad.~~

30. (withdrawn - currently amended) The integrated circuit chip ~~component~~ according to claim 29, wherein said polymer layer comprises polyimide.

31. (currently amended) The integrated circuit chip ~~component~~ according to claim 15 further comprising ~~a first metallization structure over said semiconductor substrate, a passivation layer over said first metallization structure, a second metallization structure over said passivation layer layer, and~~ a polymer layer over said passivation layer, ~~second metallization structure,~~ an opening in said polymer layer exposing said first metal pad. ~~wherein said second metallization structure is provided with said first metal pad, and an opening in said polymer layer exposes said first metal pad.~~

Claims 32-39 (canceled)

40. (currently amended) A method of fabricating an integrated ~~a~~ circuit chip, ~~component~~ comprising:

providing a semiconductor substrate, a transistor in and over ~~on~~ said semiconductor substrate, multiple metal and dielectric layers over said semiconductor substrate, and ~~a first contact pad over said semiconductor substrate,~~ a passivation layer over said multiple metal and dielectric layers, ~~semiconductor substrate,~~ an opening in said passivation layer exposing ~~a top surface of said~~ a first contact pad of said multiple metal and dielectric layers, ~~and a second contact pad connected to said top surface, wherein the~~

~~position of said second contact pad from a top perspective view is different from that of said first contact pad and~~ wherein said passivation layer comprises silicon nitride; ~~and~~

forming a second contact pad over said passivation layer, wherein said second contact pad is connected to said first contact pad through said opening, and the position of said second contact pad from a top view is different from that of said first contact pad, wherein said forming said second contact pad comprises an electroplating process; and

mounting a capacitor over said passivation layer, wherein an electrode of said capacitor is directly over and connected to said second contact pad.

Claims 41-44 (canceled)

45. (previously presented) The method according to claim 40, wherein said mounting said capacitor comprises using a surface mount technology (SMT).

Claims 46 and 47 (canceled)

48. (currently amended) The method ~~integrated circuit~~ according to claim 40 further comprising forming a wirebond over said semiconductor substrate.

49. (currently amended) The method according to claim 40, wherein said electroplating process comprises electroplating gold. ~~forming said second contact pad comprises depositing gold.~~

50. (currently amended) The method according to claim 40, wherein said electroplating process comprises electroplating copper. ~~forming said second contact pad comprises depositing copper.~~

51. (currently amended) The method according to claim 40, wherein said electroplating process comprises electroplating solder. ~~forming said second contact pad comprises depositing solder.~~

Claims 52-75 (canceled)

76. (currently amended) A method of fabricating an integrated ~~a~~ circuit chip ~~component~~ comprising:

providing a semiconductor substrate, a transistor in and over ~~on~~ said semiconductor substrate, multiple metal and dielectric layers over said semiconductor substrate, a passivation layer over said multiple metal and dielectric layers, a first contact pad over said semiconductor substrate, and a second contact pad having a portion over said passivation layer, ~~semiconductor substrate,~~ wherein said second contact pad is used to be wirebonded thereto; and

mounting a capacitor over said passivation layer, ~~semiconductor substrate,~~ wherein an electrode of said capacitor is directly over and connected to said first contact pad.

77. (currently amended) The method according to claim 76, wherein said mounting said capacitor ~~forming said first contact pad~~ comprises a printing process.

78. (currently amended) The method according to claim 76, wherein said providing ~~forming~~ said first contact pad comprises electroplating.

79. (currently amended) The method according to claim 76, wherein said providing ~~forming~~ said first contact pad comprises electroless plating.

Claim 80 (canceled)

81. (currently amended) The method according to claim 76 further comprising forming a wirebond ~~connected to~~ over said second contact pad.

82. (currently amended) The method according to claim 76, wherein said mounting said capacitor comprises using solder. ~~capacitor is connected to said first contact pad through a solder.~~

83. (currently amended) A method of fabricating an integrated ~~a~~ circuit chip ~~component~~ comprising:

providing a semiconductor substrate, a transistor in and over ~~on~~ said semiconductor substrate, multiple metal and dielectric layers over said semiconductor substrate, and a passivation layer over said multiple metal and dielectric layers; ~~a power bus over said semiconductor substrate, and a ground bus over said semiconductor substrate; and~~

forming power and ground metal structures over said passivation layer, wherein said forming said power and ground metal structures comprises depositing a copper layer; and

mounting a capacitor over said passivation layer, ~~semiconductor substrate,~~ wherein said mounting said capacitor comprises a printing process, and wherein said capacitor comprises a first electrode ~~is~~ connected to said power metal structure, and a second electrode connected to said ground metal structure. ~~buses.~~

Claims 84-87 (canceled)

88. (previously presented) The method according to claim 83 further comprising forming a wirebond over said semiconductor substrate.

89. (currently amended) The method according to claim 83, wherein said mounting said capacitor comprises using solder. ~~is connected to said power and ground buses through multiple solder connections.~~

90. (new) The method according to claim 83, wherein said passivation layer comprises silicon nitride.

91. (new) The integrated circuit chip according to claim 1, wherein said passivation layer comprises silicon nitride.

92. (new) The integrated circuit chip according to claim 1 further comprising a contact pad over said semiconductor substrate, an opening in said passivation layer exposing said contact pad, and a wirebond on said contact pad.

93. (new) The integrated circuit chip according to claim 1 further comprising a first contact pad over said semiconductor substrate, an opening in said passivation layer exposing said first contact pad, a second contact pad on said first contact pad, and a wirebond on said second contact pad.

94. (new) The integrated circuit chip according to claim 1 further comprising a contact pad over said semiconductor substrate and connected to said capacitor through said ground metal structure, and a wirebond on said contact pad.

95. (new) The integrated circuit chip according to claim 1 further comprising a contact pad over said passivation layer, and a wirebond on said contact pad.

96. (new) The integrated circuit chip according to claim 1, wherein said ground metal structure further comprises a nickel layer over said copper layer.

97. (new) The integrated circuit chip according to claim 1 further comprising a polymer layer over said power and ground metal structures, a first opening in said polymer layer exposing said power metal structure, a second opening in said polymer layer exposing said ground metal structure, said first solder connection connecting said capacitor to said

power metal structure through said first opening, said second solder connection connecting said capacitor to said ground metal structure through said second opening.

98. (new) The integrated circuit chip according to claim 9, wherein said capacitor comprises a decoupling capacitor.

99. (new) The integrated circuit chip according to claim 9, wherein said passivation layer comprises silicon nitride.

100. (new) The integrated circuit chip according to claim 14, wherein said second contact pad comprises a nickel layer over said copper layer.

101. (new) The integrated circuit chip according to claim 15, wherein said capacitor comprises a decoupling capacitor.

102. (new) The integrated circuit chip according to claim 15 further comprising a polymer layer over said passivation layer, an opening in said polymer layer exposing said second metal pad.

103. (new) The integrated circuit chip according to claim 102, wherein said polymer layer comprises polyimide.

104. (new) The integrated circuit chip according to claim 15 further comprising a metallization structure over said passivation layer and connected to a third metal pad of said multiple metal and dielectric layers exposed by an opening in said passivation layer, wherein said capacitor is connected to said second metal pad through said metallization structure.

105. (new) The method according to claim 40, wherein said capacitor comprises a decoupling capacitor.

106. (new) The method according to claim 76, wherein said capacitor comprises a decoupling capacitor.

107. (new) The method according to claim 76, wherein said passivation layer comprises silicon nitride.